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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,261	YODER, MICHAEL E.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *10-12,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/791,261 has a total of 20 claims pending in the application, there are 3 independent claims and 17 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted March 2, 2004 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of Information Disclosure Statement dated March 2, 2004 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: **Claims 14 and 15** disclose the multiprocessor operating systems comprising UNIX and Windows respectively. However, Applicant's discloses, "The computing system 100 may employ any suitable operating system ("OS") to control and direct its operations. One particular implementation employs the HP-UX OS available from the Hewlett Packard Company. However, the invention is not so limited to that particular OS. In accordance with an embodiment of the invention, the operating system supports multi-threaded processes." in line 31, pg. 4 – line 3, pg. 5 of the specification. This statement fails to properly identify the specific OS's as stated in claims 14 and 15 and therefore fails to provide proper antecedent basis for the claimed subject matter.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Default Locality Selection For Memory Objects Based On Determining The Type Of A Particular Memory Object."

6. On page 7, line 1 the phrase "page fault hander" should read "page fault handler."

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-8 and 19-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

9. **As per claims 1-8**, these claims fail to produce a tangible result. The method as claimed in independent claim 1 is merely a determination (which is nothing more than a thought or computation within a processor) followed by a selection. However, the selecting the default locality is not a physical step that in turn produces a physical and tangible result, but rather an abstract step (i.e. mentally performed step) failing to provide a tangible result. Therefore, claims 1-8 are directed to non-statutory subject matter.

10. **As per claims 19-20**, the Applicant claims an operating system in the preamble of the claim, however, that is no more than a software system, per se, thus lacking hardware necessary to realize the underlying functionality. Therefore, claims 19-20 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. **Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** As stated in MPEP § 2173.05(u), if the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. In fact, the value of a trademark would be lost to the extent that it became descriptive of a product, rather than used as an identification of a source or origin of a product. Thus, the use of a trademark or trade name in a claim to identify or describe a material or product would not only render a claim indefinite, but would also constitute an improper use of the trademark or trade name.

13. **As per claim 14**, the claim recites the phrase "UNIX operating system." UNIX™ is a registered trademark of The Open Group and is used as a limitation to identify or describe particular a particular operating system, thus, yielding the scope of this claim uncertain.

14. **As per claim 15**, the claim recites the phrase "Windows operating system." WINDOWS™ is a registered trademark of Microsoft Corporation and is used as a limitation to identify or describe particular a particular operating system, thus, yielding the scope of this claim uncertain.

15. **Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** As stated in MPEP 2173.05(b) E., the addition of the word "type" to an otherwise definite expression extends the scope of the expression so as to render it indefinite.

16. **As per claim 14**, the claim recites the phrase "a type of UNIX operating system", thus extending the scope of the expression so as to render it indefinite.

17. **As per claim 15**, the claim recites the phrase "a type of Windows operating system", thus extending the scope of the expression so as to render it indefinite.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 9, 13, and 16 are rejected under 35 U.S.C. 103(a) as being obvious over Bordaz et al. (U.S. Patent 6,272,612) in view of Noel (U.S. Patent 6,516,342).

20. **As per claim 9**, Bordaz discloses a multiprocessor computing system (col. 2, lines 27-28; Fig. 2, element 1'), the system comprising:

multiple symmetric multiprocessing (SMP) nodes (col. 2, lines 29-32; Fig. 2, elements Ma and Mb); *It should be noted that "module" is analogous to "node."*

multiple central processing units (CPUs) at each SMP node (col. 2, lines 37-40; Fig. 2, elements 10a-13a and 10b-13b);

a memory control unit at each SMP node which is coupled to each CPU at that SMP node (col. 2, lines 40-46; Fig. 2, elements La, Lb, 14a, 14b, 15a, 15b, and 2). *It should be noted that the access lines La and Lb are couple CPUs 10a-13a and 10b-13b with main memories 14a and 14b. The main memories are in turn coupled to the remote cache memories 15a and 15b via a bus. Lastly, the remote cache memories are coupled to the control circuits in link 2 which couples modules Ma and Mb.*

shared memory at each SMP node which is accessible by way of the memory control unit at that SMP node (col. 2, lines 37-40 and 55-58; Fig. 2, elements 14a and 14b); *It should be noted that "main memories 14a and 14b" are each analogous to "shared memory."*

an operating system running on the CPUs (col. 2, lines 59-62);

and a virtual memory (VM) fault handler within the operating system (col. 7, lines 12-15; col. 7, line 66 – col. 8, line 1), *It should be noted that "handler H" is analogous to "virtual memory handler."*

wherein the shared memory includes both local memory and interleaved memory (col. 8, lines 34-37 and 60-64), *It should be noted that "allocating locations in physical memory which may be distributed throughout the entire memory Mem" is analogous to an "interleaved memory" configuration.*

and wherein the VM fault handler executes instructions to provide intelligent default locality selection for memory objects requested by a process running on a CPU

(col. 8, lines 27-42; Fig. 6b). *It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify what "intelligent default locality selection for memory objects" specifically entails. Bordaz discloses that the handler determines the type of page fault and based on two parameters and predefined rules allocates locations in physical memory. Examiner interprets this to be analogous to "intelligent default locality selection for memory objects."*

Bordaz does not expressly disclose a switching system coupled to the memory control units so as to interconnect the multiple SMP nodes

Noel discloses a switching system coupled to the memory control units so as to interconnect the multiple SMP nodes (col. 6, lines 24-29 and 37-43; Fig. 1, element 116). *It should be noted that "I/O processor" is analogous to "memory control unit."*

Bordaz and Noel are analogous art because they are from the same field of endeavor, that being SMP systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Noel's switches inside Bordaz's NUMA data processing system.

The motivation for doing so would have been because switch technology, rather than bus technology, is employed to connect building block components in order to achieve the improved bandwidth and to allow for non-uniform memory architectures (NUMA) (Noel, col. 6, lines 33-36).

Therefore, it would have been obvious to combine Bordaz and Noel for the benefit of obtaining the invention as specified in claim 9.

21. **As per claim 13**, Noel discloses the switching system includes multiple switches interconnected together (col. 6, lines 37-41). *It should be noted that all the "hardware switches (plural implies multiple switches)" are interconnected by "line 122."*

22. **As per claim 16**, Bordaz discloses access time to the interleaved memory is approximately equal for each CPU in the multiprocessor system (col. 1, lines 21-26). *It should be noted that since interleaved memory is present is all shared memories for each separate module (see claim 9 citation) it follows that each CPU within any module has an approximately equal access time to the shared memory (and therefore interleaved memory) as any other CPU within the same module.*

23. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being obvious over Rogers et al. (U.S. Patent 6,970,990) in view of Bordaz.

24. **As per claim 19**, Rogers discloses an operating system for a multiprocessor computing system (col. 5, lines 11-13 and 35-36), the operating system comprising:

a virtual memory manager configured for extending a memory space beyond limits of a physical address space (col. 1, lines 14-16 and 40-43; col. 5, line 67 – col. 6, line 5; Fig. 2, element 250).

and a page fault handler to interrupt execution of the virtual memory manager when a page fault occurs (col. 8, lines 7-18).

Rogers does not expressly disclose the page fault handler is configured to provide intelligent default locality selection for memory objects.

Bordaz discloses the page fault handler is configured to provide intelligent default locality selection for memory objects (col. 8, lines 27-42; Fig. 6b). *See citation note for the last limitation of claim 9 above.*

Rogers and Bordaz are analogous art because they are from the same field of endeavor, that being virtual addressing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bordaz's handler within Roger's virtual memory manager.

The motivation for doing so would have been to carry out memory allocation as a function of a the profile specific to each application by implementing a set of allocation rules which take this profile into account, among which a search is automatically performed upon each page fault detected, in order to determine which one must be executed for the physical memory allocation, thus making it possible to optimize the memory accesses as a function of this parameter and also offering a significant improvement relative to prior art, particularly in terms of better performance and great flexibility (Bordaz, col. 3, lines 56-62; col. 4, lines 1-7).

Therefore, it would have been obvious to combine Rogers and Bordaz for the benefit of obtaining the invention as specified in claim 19.

25. **As per claim 20**, Bordaz discloses the intelligent default locality selection is configured to choose from a set of choices including local memories residing at each node of the system and interleaved memory which is striped to reside on multiple nodes of the system (col. 8, lines 27-42 and 57-67; Fig. 6b). *See citation note for the last limitation of claim 9 above.*

26. Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over Bordaz in view of Noel as applied to claim 9 above, and in further view of Numeric Quest Inc., "Multithreading – Definitions and Guideliness", hereafter "Numeric."

27. Bordaz/Noel discloses the operating system comprises a type of UNIX operating system (Bordaz, col. 6, line 33-34).

Bordaz/Noel does not expressly disclose the operating system supports multi-threaded processes.

Numeric discloses an operating system comprises a type of UNIX operating system, and wherein the operating system supports multi-threaded processes (pg. 3, lines 20-22).

Bordaz/Noel and Numeric are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Numeric's UNIX operating system capable of multi-threading within Bordaz/Noel's SMP system.

The motivation for doing so would have been to improve application responsiveness, use multiprocessors more efficiently, improve program structure, use fewer system resources, and improve performance (Numeric, pg. 2, lines 1-25).

Therefore, it would have been obvious to combine Bordaz/Noel and Numeric for the benefit of obtaining the invention as specified in claim 14.

28. Claim 15 is rejected under 35 U.S.C. 103(a) as being obvious over Bordaz in view of Noel as applied to claim 9 above, and in further view of Ruediger R. Asche, "Multithreading for Rookies", hereafter "Asche."

29. Bordaz/Noel disclose all the limitations of claim 15 except the operating system comprises a type of Windows operating system, and wherein the operating system supports multi-threaded processes.

Asche discloses the operating system comprises a type of Windows operating system, and wherein the operating system supports multi-threaded processes (pg. 1, Abstract, lines 1-8).

Bordaz/Noel and Asche are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Asche's Windows operating system capable of multi-threading within Bordaz/Noel's SMP system.

The motivation for doing so would have been to help applications respond better and perform better whenever there is a true case of background processing (that is, a sequence of code that does not require user interaction and can run independent of whatever happens in the foreground) (Asche, pg. 4, lines 3-5).

Another motivation for doing so would have been because any asynchronous work that needs to be done (such as polling on a serial port) probably works much better in a dedicated thread than competing with the foreground task in the same thread of execution (Asche, pg. 4, lines 5-7).

Therefore, it would have been obvious to combine Bordaz/Noel and Asche for the benefit of obtaining the invention as specified in claim 15.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

30. **Claims 1-8** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 101, set forth in this Office action.

31. The primary reasons for allowance of **claims 1-8** in the instant application is the combination with the inclusion in these claims that "**determining whether the memory object comprises a shared-memory object; selecting the default locality to be within interleaved memory of the system if the memory object comprises said shared-memory object.**" The prior art of record neither anticipates nor renders obvious the above recited combination.

32. **Claims 10-12 and 17-18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33. The primary reasons for allowance of **claims 10-12 and 17-18** in the instant application is the combination with the inclusion in these claims that "**said instructions executed by the VM fault handler (a) determine whether the memory object**

comprises a shared-memory object, and (b) select the default locality to be within the interleaved memory of the system if the memory object comprises said shared-memory object." The prior art of record neither anticipates nor renders obvious the above recited combination.

34. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,699,539 discloses a virtual memory system and method enable a computer system to use a virtual memory address space larger than the size of physical primary memory while swapping few, if any, pages out to secondary memory.

2. U.S. Patent 6,516,342 discloses a method and apparatus for extending memory using a memory server.

3. U.S. Patent 6,567,900 discloses efficient address interleaving with simultaneous multiple locality options.

4. U.S. Patent 6,598,130 discloses a technique for referencing distributed shared memory locally rather than remotely.

5. U.S. Patent 6,871,219 discloses a distributed shared memory multiprocessor computer system utilizing page placement policies to reduce data access latencies in which pages of memory are allocated to nodes in the distributed shared memory multiprocessor computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Assistant Examiner
Art Unit 2185
March 29, 2006

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SUPERVISORY PATENT EXAMINER